CLAIM AMENDMENT:

Please amend claims 18, 32 and 36 as follows:

Claim 1 (previously presented): A multi-chip package type semiconductor device, comprising:

an insulating substrate having thereon a first conductive pattern and a second conductive pattern;

a first semiconductor chip having a first internal circuit on the insulating substrate, the first semiconductor chip having a first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad, and the conductive relay pad including a first area and a second area, which is different from the first area;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a first bonding wire connecting the first terminal pad to the first conductive pattern;

a second bonding wire connecting the second conductive pattern to the conductive relay pad in the first area; and

a third bonding wire connecting the conductive relay pad in the second area to the second terminal pad;

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 2 (original): A multi-chip package type semiconductor device, as claimed in claim 1, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

Claim 3 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 2, further comprising a first metal bump formed on the conductive relay pad in the first area and a second metal bump formed on the second terminal pad, wherein a first bond as a beginning connection of the first bonding wire is preformed at the first terminal pad and a second bond as an ending connection of the first bonding wire is made at the first conductive pattern, wherein a first bond as a beginning connection of the second bonding wire is preformed at the second conductive pattern and a second bond as an ending connection of the second bonding wire is made at the first metal bump, and wherein a first bond as a beginning connection of the third bonding wire is preformed at the conductive relay pad in the second area and a second bond as an ending connection of the third bonding wire is made at the second metal bump.

Claim 4 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 2, further comprising a metal bump formed on the conductive relay pad in the second area, wherein a first bond as a beginning connection of the first bonding wire is preformed at the first terminal pad and a second bond as an ending connection of the first bonding wire is made at the first conductive pattern, wherein a first bond as a beginning connection of the second bonding wire is

preformed at the conductive relay pad in the first area and a second bond as an ending connection of the second bonding wire is made at the second conductive pattern, and wherein a first bond as a beginning connection of the third bonding wire is preformed at the second terminal pad and a second bond as an ending connection of the third bonding wire is made at the metal bump.

Claim 5 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip, wherein a distance from the side of the first semiconductor chip to the first area is almost the same as that from the side of the first semiconductor chip to the second area.

Claim 6 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

Claim 7 (original): A multi-chip package type semiconductor device, as claimed in claim 6, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

Claim 8 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip, wherein a distance from the side of the first semiconductor chip to the first area is almost the same as that from the side of the first semiconductor chip to the second area.

Claim 9 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

Claim 10 (original): A multi-chip package type semiconductor device, as claimed in claim 9, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

Claim 11 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 3, wherein the first metal bump is spaced apart from the first bond of the third bonding wire, but is electrically connected to the first bond of the third bonding wire via the conductive relay pad.

Claim 12 (previously presented): A multi-chip package type semiconductor

device, as claimed in claim 4, wherein the metal bump is spaced apart from the first bond of the second bonding wire, but is electrically connected to the first bond of the second bonding wire via the conductive relay pad.

Claim 13 (previously presented): A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a first terminal pad and a conductive relay pad, the conductive relay pad including a first area and a second area, which is different from the first area;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a second terminal pad, connected to the conductive relay pad in the second area;

a first internal terminal connected to the first terminal pad; and

a second internal terminal connected to the conductive relay pad in the first area.

Claim 14 (original): A multi-chip package type semiconductor device, as claimed in claim 13, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

Claim 15 (original): A multi-chip package type semiconductor device, comprising:

an insulating substrate having a first and second conductive patterns thereon;

a first semiconductor chip on the insulating substrate, the first semiconductor chip having a first internal circuit, a first terminal pad connecting to the first internal

circuit and a conductive relay pad isolated from the first terminal pad;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a first bonding wire connecting the first terminal pad to the first conductive pattern;

a second bonding wire connecting the second conductive pattern to the conductive relay pad; and

a third bonding wire connecting the conductive relay pad to the second terminal pad;

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 16 (original): A multi-chip package type semiconductor device, as claimed in claim 15, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

Claim 17 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 16, further comprising a first metal bump formed on the conductive relay pad and a second metal bump formed on the second terminal pad, wherein a first bond as a beginning connection of the first bonding wire is preformed at the first terminal pad and a second bond as an ending connection of the first bonding wire is made at the first conductive pattern, wherein a first bond as a

beginning connection of the second bonding wire is preformed at the second conductive pattern and a second bond as an ending connection of the second bonding wire is made at the first metal bump, and wherein a first bond as a beginning connection of the third bonding wire is preformed at the first metal bump and a second bond as an ending connection of the third bonding wire is made at the second metal bump.

Claim 18 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 16, further comprising a metal bump formed on the conductive relay pad, wherein a first bond as a beginning connection of the first bonding wire is preformed at the first terminal pad and a second bond as an ending connection of the first bonding wire is made at the first conductive pattern, wherein a first bond as a beginning connection of the second bonding wire is preformed at the second conductive pattern and a second bond as an ending connection of the second bonding wire is made at the metal bump, and wherein a first bond as a beginning connection of the third bonding wire is preformed at the second terminal pad and a second bond as an ending connection of the third bonding wire is made at the metal bump.

Claim 19 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 13, wherein the first area and the second area are located along a side of the first semiconductor chip.

Claim 20 (previously presented): A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a first conductive portion and a second conductive portion, the second conductive portion having a first area and a second area, which is different from the first area;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a third conductive portion, connected to the second conductive portion in the first area;

a first internal terminal connected to the first conductive portion; and

a second internal terminal connected to the second conductive portion in the second area.

Claim 21 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are located along a side of the first semiconductor chip.

Claim 22 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 20, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

Claim 23 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are spaced from each other.

Claim 24 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 20, further comprising:

a bump formed on the second conductive portion in the second area; and

a first wire, the first wire having one end connected to the second terminal and the other end connected to the bump.

Claim 25 (previously presented): A multi-chip package type semiconductor device, comprising:

an insulating substrate;

a first conductive pattern formed on the insulating substrate;

a first semiconductor chip mounted on the insulating substrate;

a second conductive pattern formed on the first semiconductor chip, the second conductive pattern having a first area and a second area, which is different from the first area;

a second semiconductor chip mounted on the first semiconductor chip;

a third conductive pattern formed on the second semiconductor chip;

a first wire connected between the first area of the second conductive pattern and the third conductive pattern; and

a second wire connected between the second area of the second conductive pattern and the first conductive pattern.

Claim 26 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 25, wherein the first area and the second areas are located along a side of the first semiconductor chip.

Claim 27 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 25, further comprising:

a first bump formed on the first area of the second conductive pattern; and

a second bump formed on the third conductive pattern,

wherein the first wire is connected to the first area through the first bump and the second wire is connected to the third conductive pattern through the second bump.

Claim 28 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 25, wherein the first area and the second area are spaced each other.

Claim 29 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 1, further comprising a plurality of first terminal pads and a plurality of conductive relay pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned.

Claim 30 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 1, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claim 31 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 13, further comprising a plurality of first terminal pads and a plurality of conductive relay pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned.

Claim 32 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 13, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to [[the]] a side of the first semiconductor chip.

Claim 33 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 15, further comprising a plurality of first terminal pads and a plurality of conductive relay pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned.

Claim 34 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 15, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claim 35 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 20, further comprising a plurality of first conductive portions and a plurality of second conductive portions, wherein each first conductive portion and each second conductive portion are alternatively aligned.

Claim 36 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first conductive portion is rectangularly-shaped, and a side of the first conductive portion is parallel to [[the]] a side of the first semiconductor chip.